This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-107. (cancelled)

108. (currently amended) A method of fabricating a semiconductor die, comprising:

forming a test structure on the semiconductor die, wherein at least a portion of the test structure includes a dummy structure in a top conductive layer, wherein the dummy structure of the test structure serves as both a dummy structure and a part of a voltage contrast structure, wherein serving as a dummy structure is defined as the dummy structure of the test structure being part of a plurality of dummy structures that are distributed within empty spaces of the semiconductor die to facilitate an even polishing of a surface of the semiconductor die, and wherein only a portion of the dummy structures each serve as a voltage contrast structure while the other portion of dummy structures do not each serve as a voltage contrast structure; and

performing voltage contrast testing on the test structure that serves as both a dummy structure and a voltage contrast structure to detect electrical defects within the test structure.

109. (previously presented) The method of claim 108, wherein the test structure comprises:

a substrate; and

at least one contact which couples the dummy structure to the substrate.

110. (previously presented) The method of claim 109, wherein the test structure further comprises:

a first conductive layer portion over the substrate and underneath the dummy structure;

a first isolation layer between the first conductive layer portion and the substrate;

a second isolation layer between the first conductive layer portion and the dummy structure;

a first contact for coupling the substrate to the first conductive layer portion; and

a second contact for coupling the first conductive layer portion to the dummy structure.

111. (previously presented) The method of claim 110, wherein at least one of the first and second contacts is a redundant type contact.

112. (previously presented) The method of claim 110, wherein the voltage contrast testing comprises:

scanning an electron beam over the dummy structure to thereby cause electron emission from the dummy structure; and

determining that the test structure has a defect between the substrate and the dummy structure when electron emission is impeded from the dummy structure.

113. (previously presented) The method of claim 112, wherein the defect is an open defect.

114. (previously presented) The method of claim 108, further comprising:

forming a plurality of test structures on the semiconductor die, wherein at least a portion of each test structure includes a dummy structure, wherein the test structures permit voltage contrast testing and wherein some of the test structures also include contacts for coupling its dummy structure to a substrate of the semiconductor die and others of the test structures remain floating; and

performing voltage contrast testing on the test structures to detect electrical defects within the test structures.

115. (previously presented) The method of claim 114, wherein the voltage contrast testing comprises:

scanning an electron beam over the dummy structures to thereby cause electron emission from the dummy structures;

determining that a particular one of the dummy structures and its associated test structure has a defect between the substrate and the dummy structure by analyzing the electron emission from the dummy structures.

116. (previously presented) The method of claim 115, wherein the defect is an open defect.

117. (previously presented) The method of claim 108, the test structure further comprising:

a first conductive layer portion underneath the dummy structure; and

a via coupling the first conductive layer portion to the dummy structure.

118. (previously presented) The method of claim 117, the test structure further comprising:

a substrate underneath the first conductive layer portion; and

a via coupling the first conductive layer portion to the substrate.

119. (previously presented) The method of claim 118, wherein the via is a redundant via.

120. (previously presented) The method of claim 118, wherein the test structure further comprises a plurality of stacked conductive layers and vias to form a multilevel test structure.

121. (previously presented) The method of claim 120, wherein at least one of the vias is a redundant via.